Understanding Intersil Hot Plug Devices

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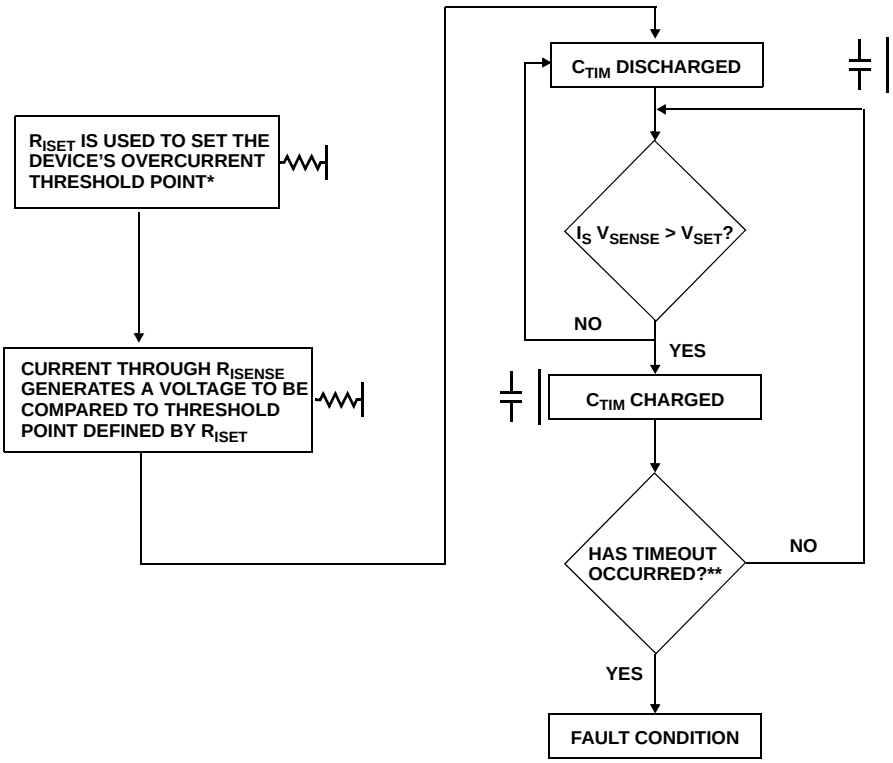
Overview

Hot Plug controllers have two primary responsibilities, control inrush currents during turn-on and control load currents to a safe pre-determined level in the event of a high current fault/short during static operation.

Devices Under Observation

- ISL6116 (+5V)
- ISL6116 (-12V)
- ISL6116 (-48V)
- ISL6115 (+12V)
- HIP1012A (+5V and +3.3V)
- ISL6173 (+3.3V and +2.5V)
- ISL6111(+12V, -12V, +3.3V, +5V)
- ISL6118 (+5V x2)
- Setting the Overcurrent Trip Point



*See respective controller datasheet for equations to select R_{ISET}

**Timeout is proportional to CTIM and varies by controller (see datasheets)

OVERCURRENT TRIP POINT OPERATION

ISL6116 (+5V)

Figures 1 and 2 show the ISL6116 in an ISL6115 high side switch application eval board. Jumper JP1 is removed from the original configuration so a +5V Power Source can be applied to B2. +12V is needed to bias the IC and is applied at B1. The overcurrent set point is 1.5A.

In Figure 3, notice the soft-start ramp up of GATE after PWRON is initiated, thus allowing the gradual ramp up of I_{LOAD}. In Figure 4, starting up into a short is shown. Upon PWRON being asserted, CTIM is immediately begins charging. The nominal time-out period is CTIM x 93kΩ . An overcurrent (OC) event occurs when the current through the sense resistor exceeds the user programmed OC threshold (see data sheet). The controller enters current regulation (CR) and capacitor CTIM begins charging. The nominal time-out period is CTIM x 93kΩ. (see Figure 5A). A transient event from 500mA to 1A occurs. PGOOD is pulled low due to a temporary undervoltage condition occurring on $+5V_{OUT}$, but CTIM stays low as a true OC event never occurs (See Figure 5B).

ISL6116 (+5V) Figures

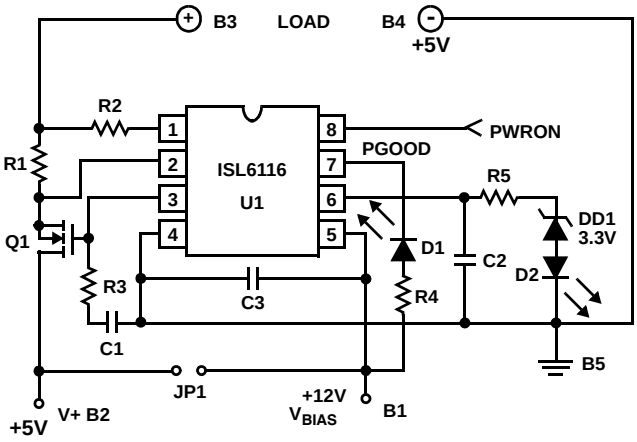


FIGURE 1. EVAL BOARD SCHEMATIC

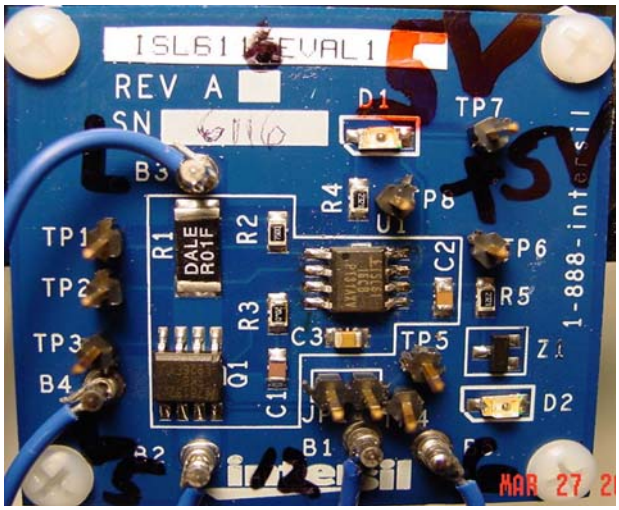


FIGURE 2. EVAL BOARD PICTURE

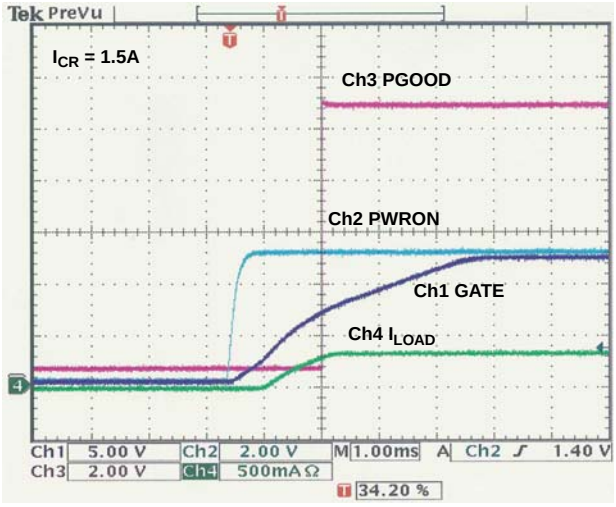


FIGURE 3. TURN ON VIA PWRON INTO NOMINAL LOAD

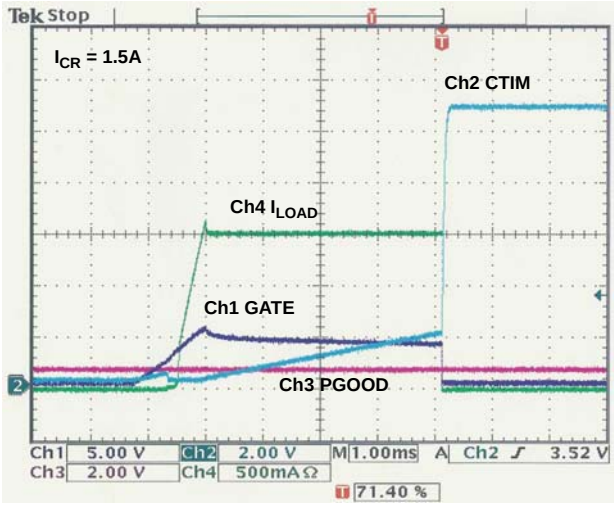


FIGURE 4. TURN ON VIA PWRON INTO SHORT

ISL6116 (+5V) Figures (Continued)

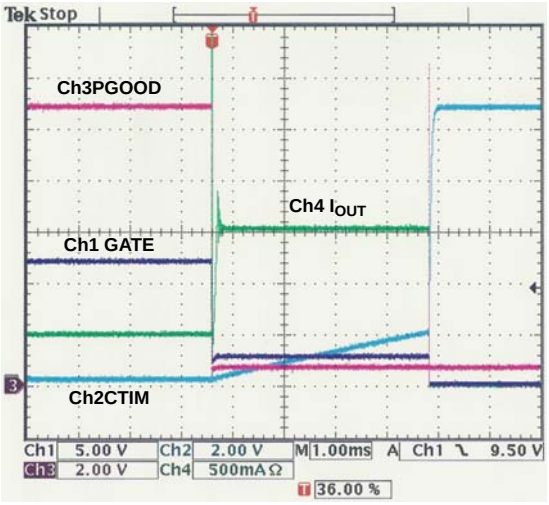


FIGURE 5A. RESPONSE TO OC DURING OPERATION

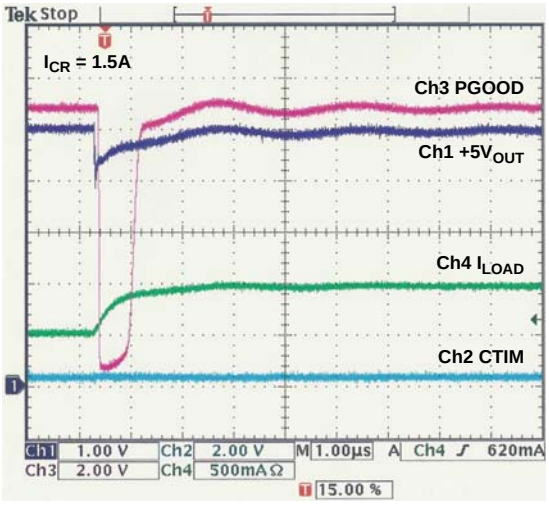


FIGURE 5B. RESPONSE TO FALSE FAULT EVENT

FIGURE 5.

ISL6116 (-12V)

Figures 6 and 7 show the ISL6116 reconfigured for -12V low side switch application. The following components were removed: RG1, R6 & R11. C2 was added (0.047µf 0805 size). In Figure 8, notice that GATE is 0V to fully enhance the FET because of -12V operation. Also note that PGOOD is disabled due to low side configuration. Upon power up, current regulation mode is entered and CTIM is immediately begins charging. The nominal time-out period is CTIM x 93kΩ, and again PGOOD is disabled (see Figure 9). An OC event occurs when the current through the sense resistor exceeds the user programmed OC threshold (see data sheet). The controller enters CR mode and capacitor CTIM begins charging. The nominal time-out period is CTIM x 93kΩ (see Figure 10).

ISL6116 (-12V) Figures

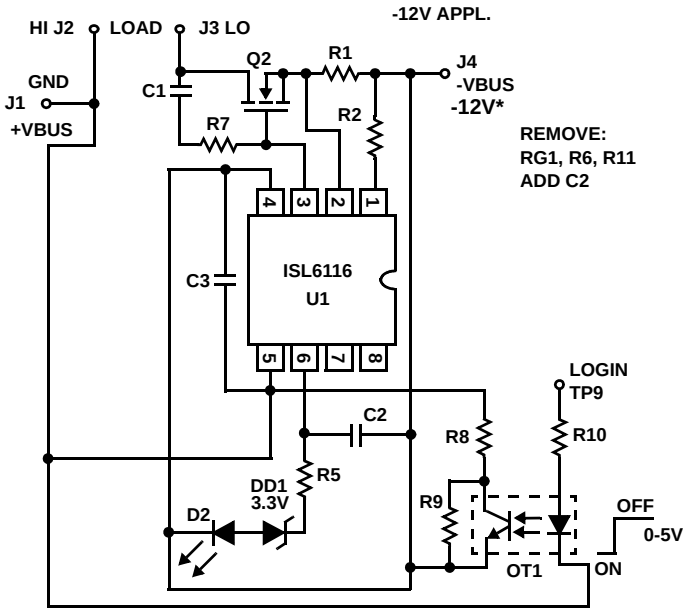


FIGURE 6. ISL6116EVAL1 NEGATIVE VOLTAGE LOW SIDE CONTROLLER

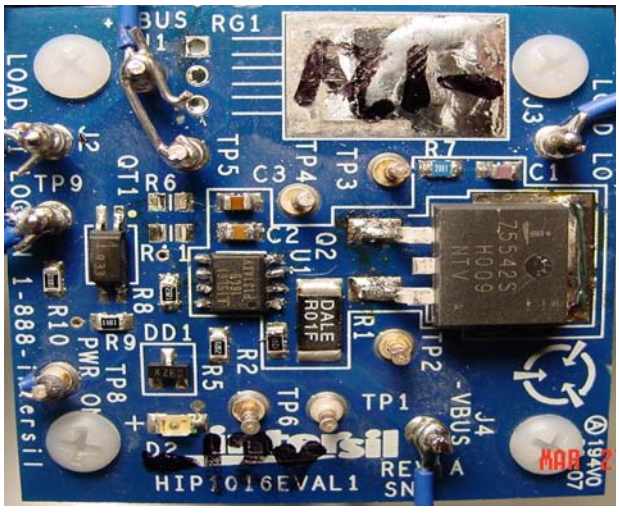


FIGURE 7. ISL6116 EVAL BOARD PICTURE

ISL6116 (-12V) Figures (Continued)

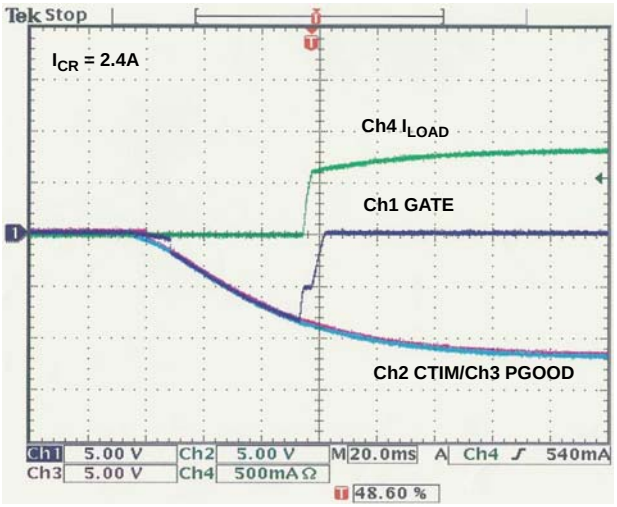


FIGURE 8. TURN ON INTO NOMINAL LOAD

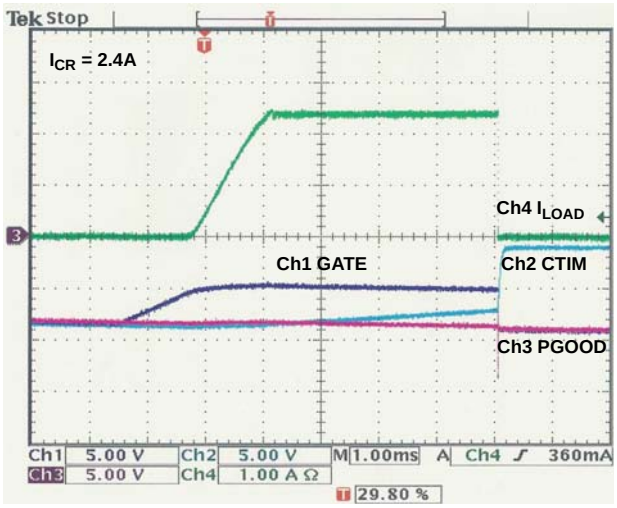


FIGURE 9. TURN ON INTO OVERCURRENT

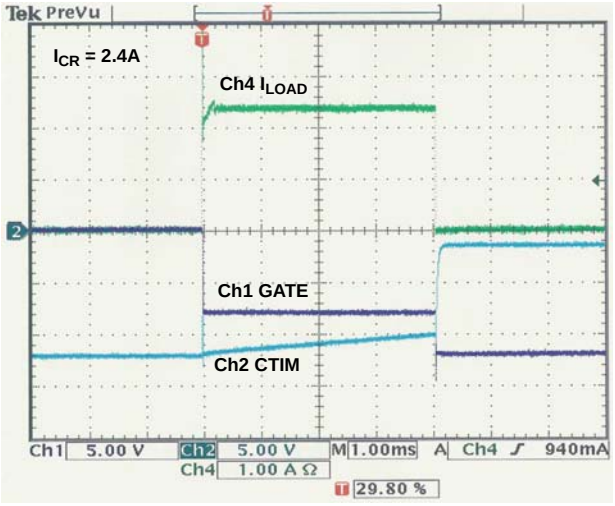


FIGURE 10. RESPONSE TO OC DURING OPERATION

ISL6116 (-48V)

Figure 11 and 12 show the ISL6116 in -48V Low Side Switch Application. The eval board uses a HIP5600 to bias the ISL6116 12V higher than the -48V. Note C2 was intentionally left empty. Tests were done at -36V to keep the power dissipated to the load low. Results would be essentially the same at -48V.

In Figure 13, notice soft-start ramp up of GATE upon LOGIN is being driven low. Keep in mind that PGOOD is disabled in low side applications. Upon an OC at turn on, GATE begins to soft-start, then attempts to regulate, then is shut down (see Figure 14). Note CTIM's behavior due to the eval board setup (C2 DNP).

In Figure 15, the load is switched from an open to 2Ω. The controller immediately pulls GATE down, CTIM up, and the load is isolated. When LOGIN is forced high, the controller shuts down (see Figure 16).

ISL6116 (-48V) Figures

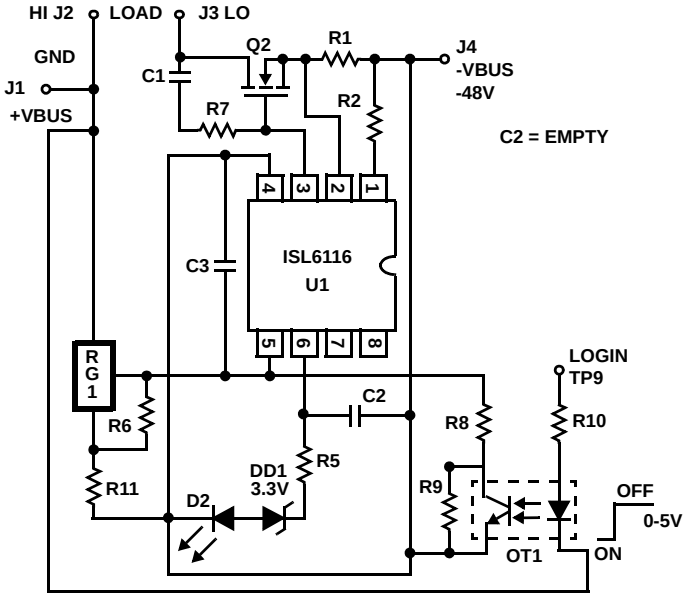


FIGURE 11. ISL6116 EVAL BOARD SCHEMATIC

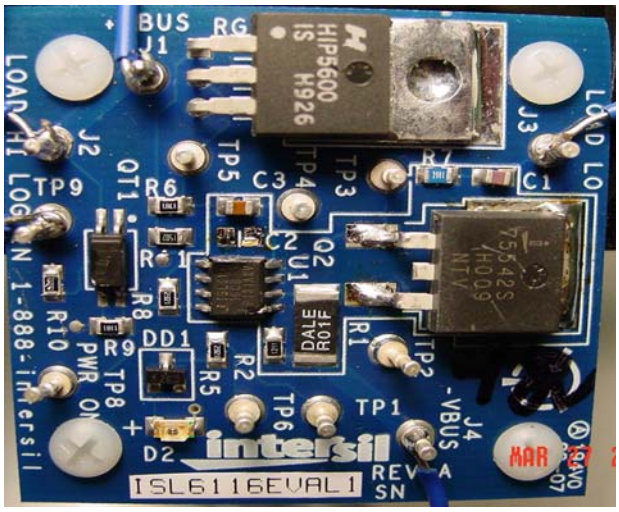


FIGURE 12. ISL6116 EVAL BOARD PICTURE

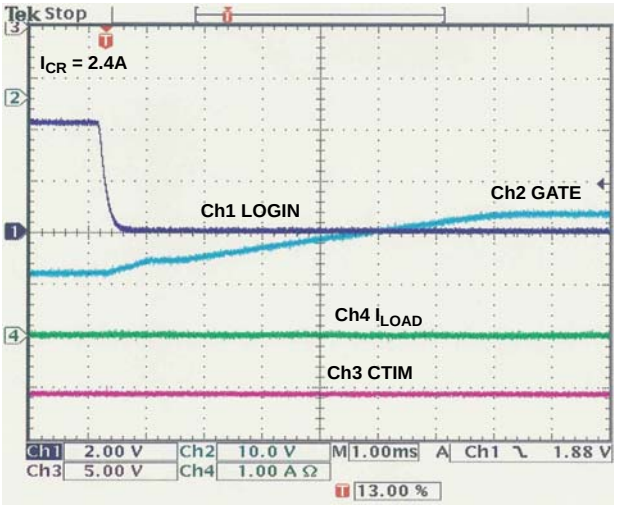


FIGURE 13. TURN ON VIA LOGIN

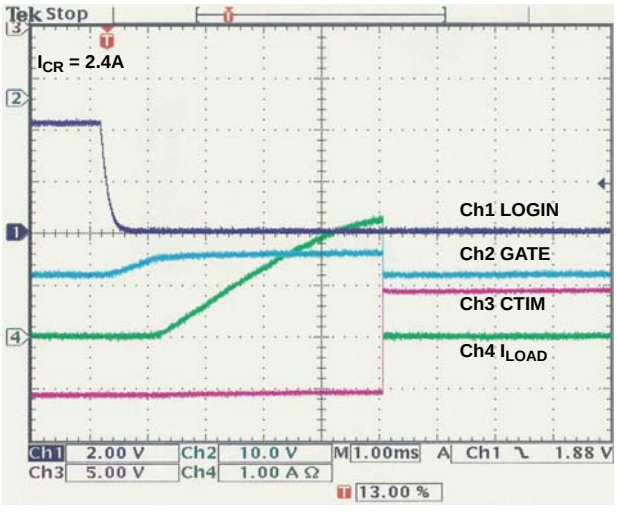


FIGURE 14. TURN ON INTO OC

ISL6116 (-48V) Figures (Continued)

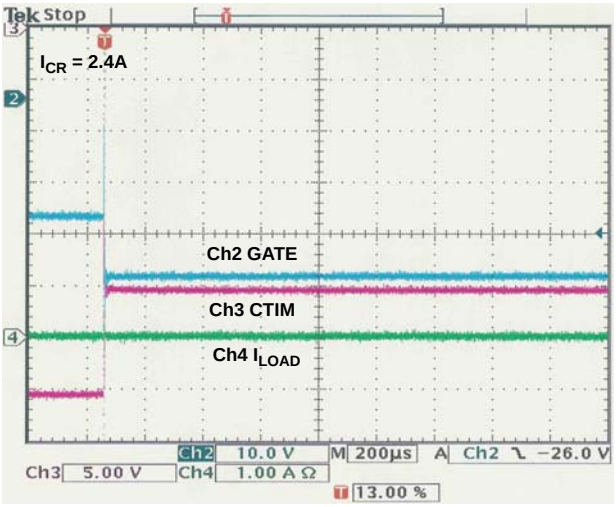


FIGURE 15. RESPONSE TO OC DURING OPERATION

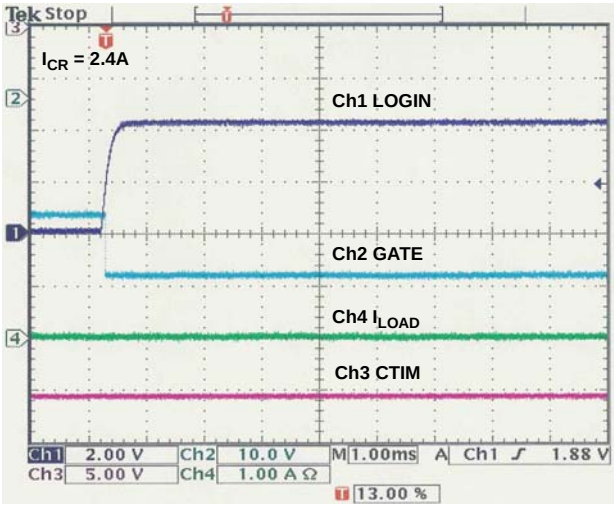


FIGURE 16. TURN OFF VIA LOGIN

ISL6115 (+12V)

Figures 17 and 18 show the ISL6115 in a +12V high side switch application.

Refer to Figures 19 and 20. After PWRON is asserted, notice the soft-start ramp of GATE to assure inrush current is limited. Observe the PGOOD delay as well.

Both Figures 21 and 22 show an OC event; Figure 21 shows turning on into a short, and Figure 22 shows a short occurring during normal operation. An OC event occurs when the current through the sense resistor exceeds the user programmed OC threshold (see data sheet). The controller enters CR mode and capacitor CTIM begins charging. The nominal time-out period is CTIM x 93kΩ.

ISL6115 (+12V) Figures

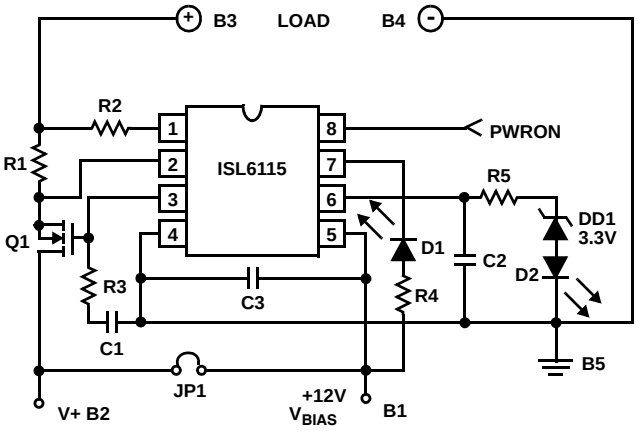


FIGURE 17. ISL6115 EVAL BOARD SCHEMATIC

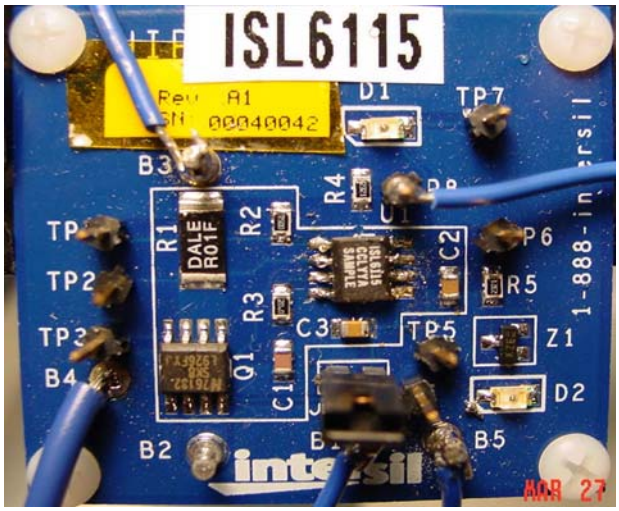


FIGURE 18. ISL6115 EVAL BOARD PICTURE

ISL6115 (+12V) Figures (Continued)

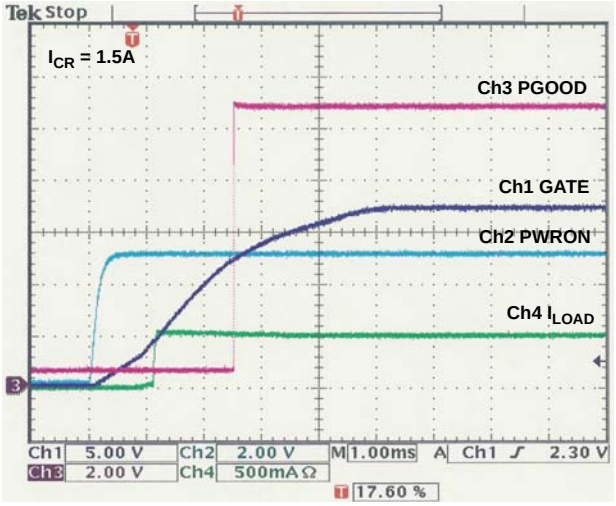


FIGURE 19. TURN ON VIA PWRON INTO NOMINAL LOAD

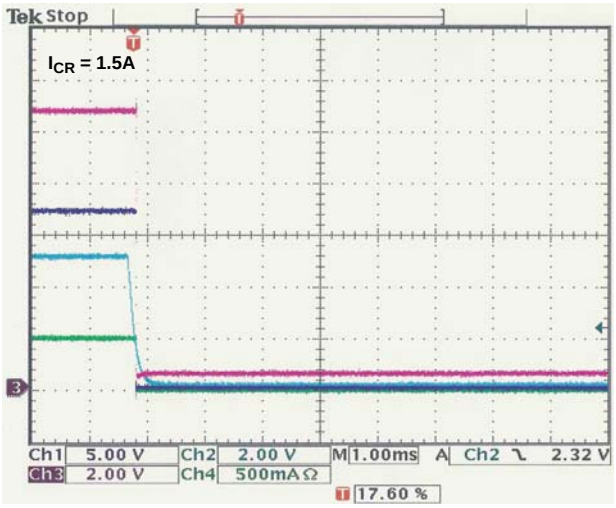


FIGURE 20. TURN OFF VIA PWRON

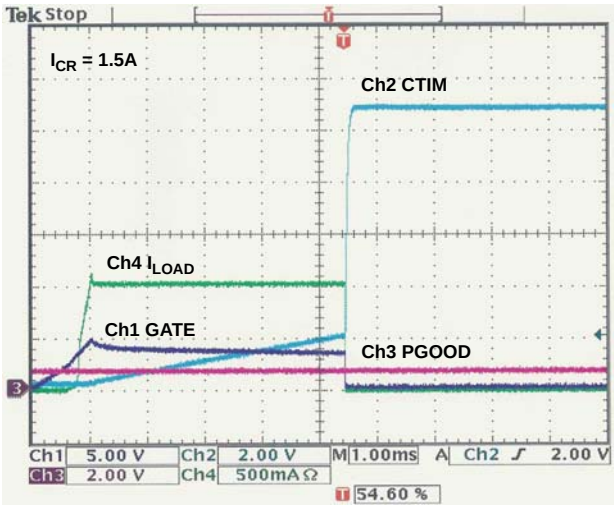


FIGURE 21. TURN ON INTO OC

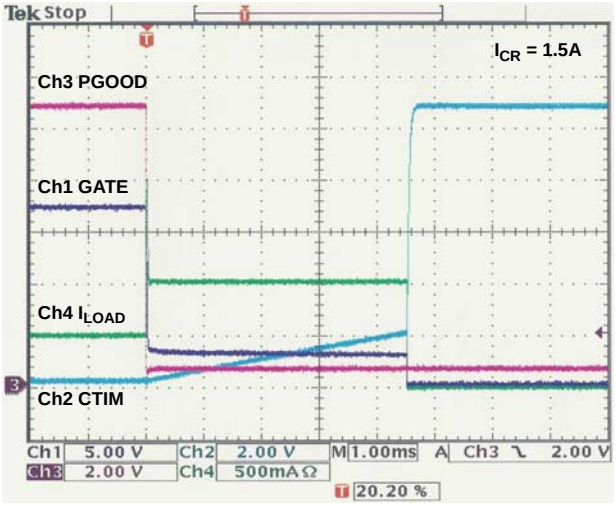


FIGURE 22. RESPONSE TO OC DURING OPERATION

HIP1012A (+5V and +3.3V)

Figures 23 and 24 show the HIP1012A dual Hot Swap controller. To configure for +3.3V and +5V, remove JP1, and apply a function generator at pin2 of JP1 for (PWRON2)'.

Figures 25 and 26 show the HIP1012A dual Hot Swap controller load card.

TABLE 1. HOT SWAP CONTROLLER LOAD CARD

3.3V LOAD	5V LOAD
00 = Off	00 = Off
01 = 1.0Ω (3.3A)	01 = 10.1Ω (0.5A)
10 = 1.8Ω (1.8A)	10 = 7.0Ω (0.7A)
11 = 0.7Ω (4.7A)	11 = 4.2Ω (1.2A)

Both Figures 27 and 28 show the same event. Figure 27 shows 5VG and Figure 28 shows $I_{3.3V}$. After $\overline{\text{PWRON2}}$ is asserted (forced low), notice the soft-start ramp of 3/12VG to assure inrush current is limited. Observe the PGOOD delay as well.

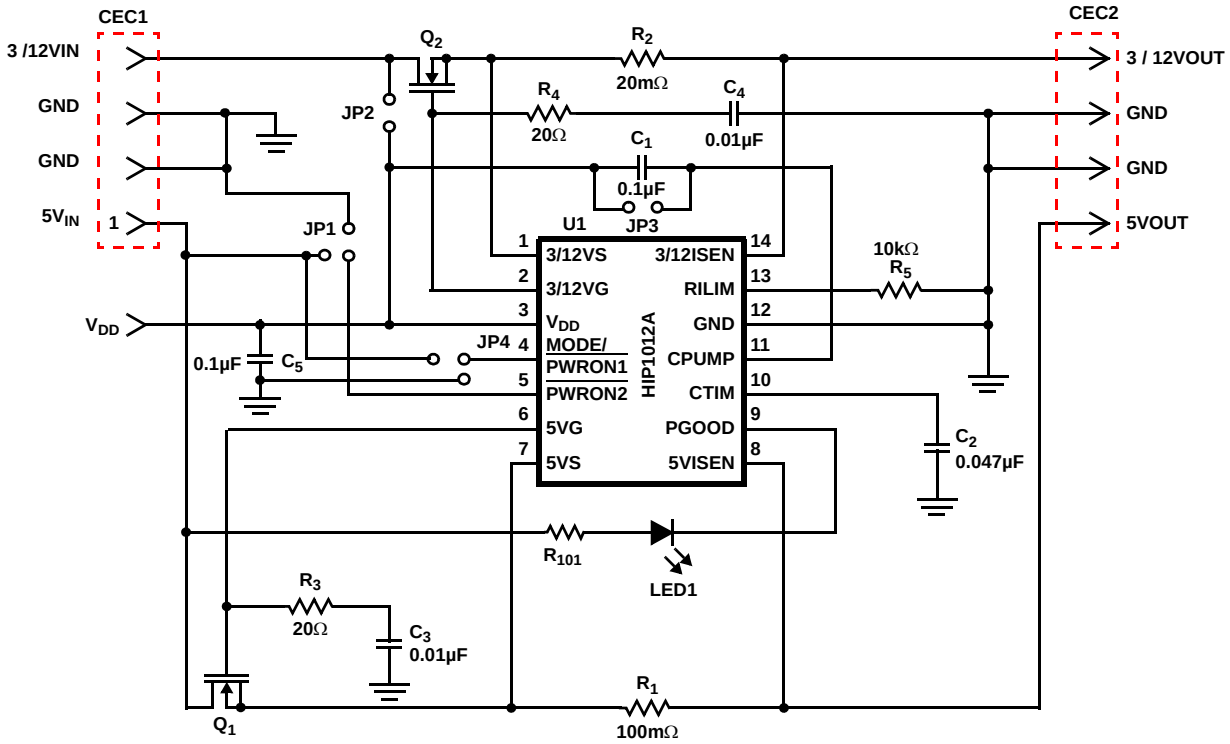
Figures 29 and 30 both show the same event. Figure 29 shows 5VG and Figure 30 shows $I_{3.3V}$. Controller is shutdown by forcing $\overline{\text{PWRON2}}$ high.

Figures 31 and 32 show turning on into an OC condition. Figure 31 shows 3/12VG and $\overline{\text{PWRON2}}$, while Figure 32 shows I_{5V} and PGOOD. An OC event occurs when the current through the sense resistor exceeds the user programmed OC threshold (see data sheet). The controller enters CR mode and capacitor CTIM begins charging. The nominal time-out period is CTIM x 200kΩ.

Both Figures 33 and 34 show an OC event. Figure 33 shows a 700mA to 1.2A load step into OC range during normal operation, while Figure 34 shows a short occurring during normal operation. Notice that in the "short condition", Figure 34, 5VG is pulled instantly to GND, then slowly ramped up.

An OC event occurs on the 5V line. Notice that the 3.3V line continues operating normally until CTIM times out and the device latches off (see Figure 35).

HIP1012A (+5V and +3.3V) Figures



Note: Test point number equals HIP1012A pin number.

FIGURE 23. HIP1012A EVAL BOARD SCHEMATIC

HIP1012A (+5V and +3.3V) Figures (Continued)

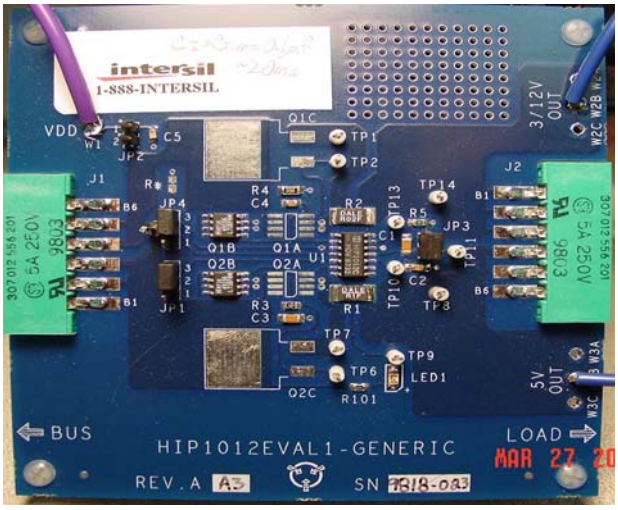


FIGURE 24. HIP1012A EVAL BOARD PICTURE

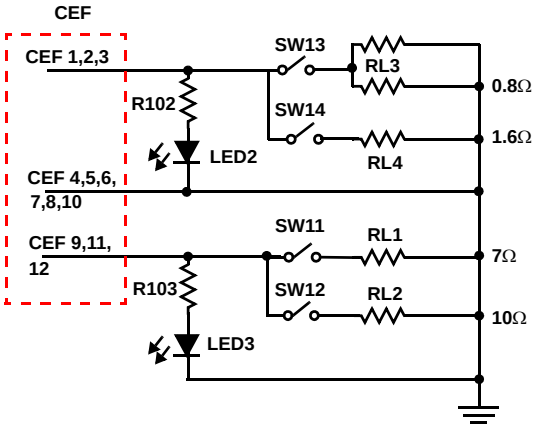


FIGURE 25. LOAD CIRCUIT SCHEMATIC

FIGURE 26. LOAD CIRCUIT EVAL BOARD PICTURE

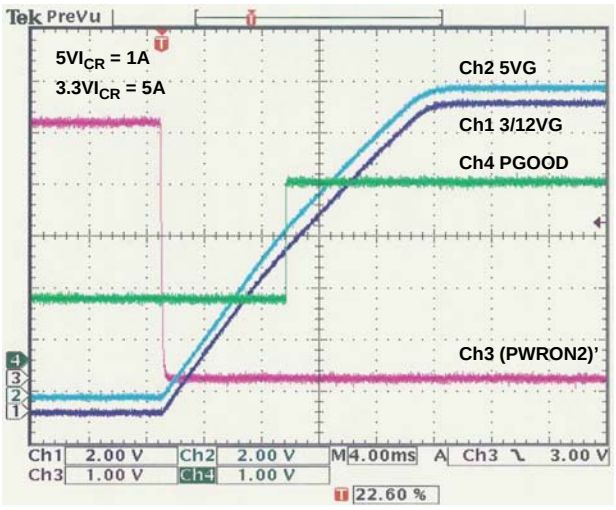


FIGURE 27. TURN ON SHOWING BOTH CHANNELS

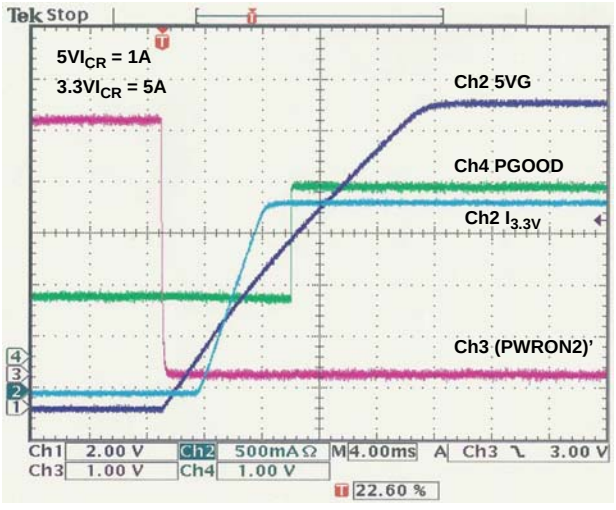


FIGURE 28. TURN ON SHOWING +3.3V DETAILS

HIP1012A (+5V and +3.3V) Figures (Continued)

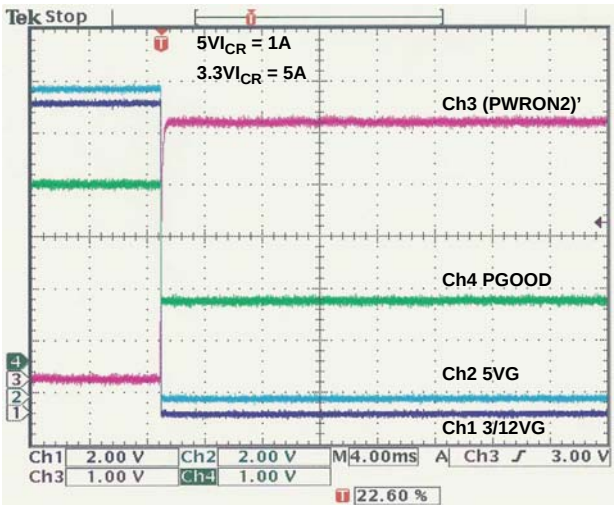


FIGURE 29. TURN OFF VIA SHOWING BOTH CHANNELS

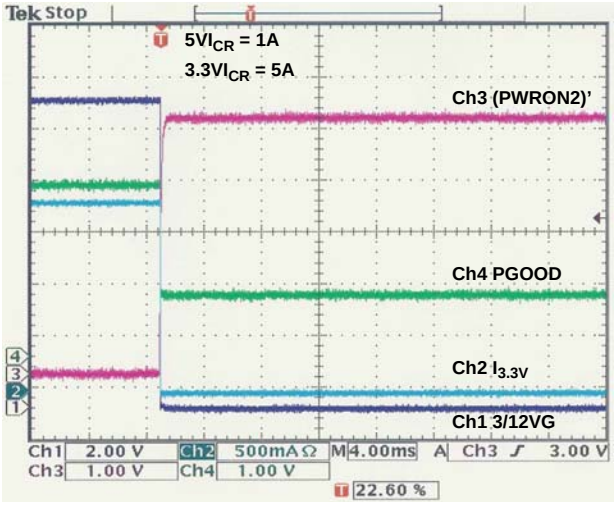


FIGURE 30. TURN OFF VIA SHOWING +3.3V DETAILS

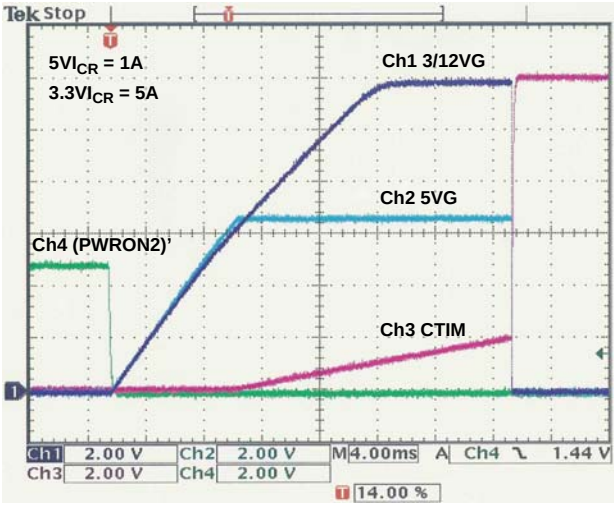


FIGURE 31. TURN ON INTO OC SHOWING BOTH CHANNELS

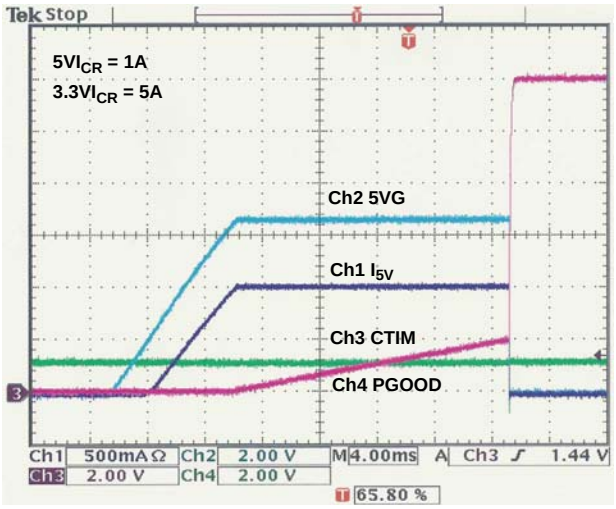


FIGURE 32. TURN ON INTO OC SHOWING +5V DETAILS

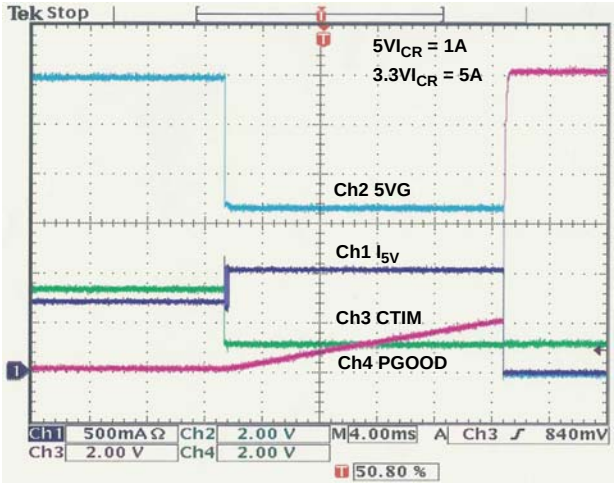


FIGURE 33. RESPONSE TO SHORT DURING OPERATION

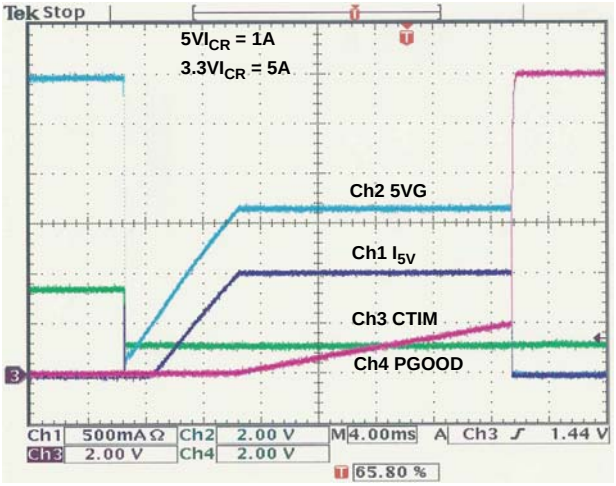


FIGURE 34. RESPONSE TO OC DURING OPERATION1

HIP1012A (+5V and +3.3V) Figures (Continued)

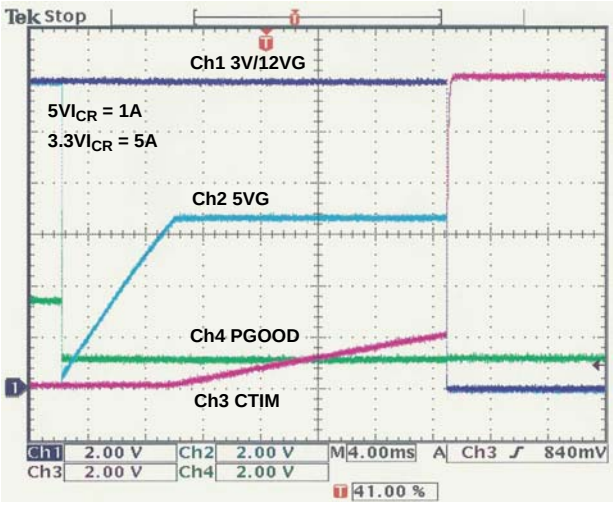
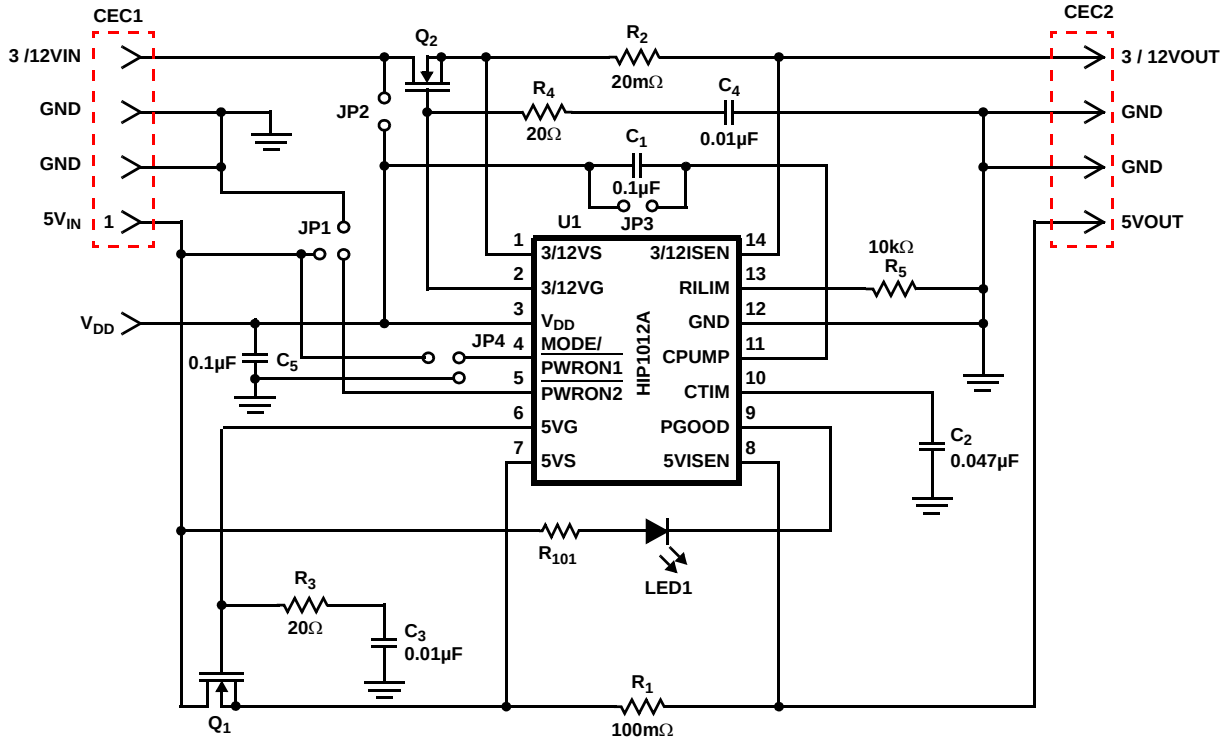


FIGURE 35. RESPONSE TO OC SHOWING BOTH CHANNELS

HIP1012A (+5V and 12V)

The HIP1012A eval board can also be configured for +5V & +12V Hot Swap control. To do this, jumpers JP3 and JP4 must be removed.

HIP1012A (+5V and 12V) Figures



Note: Test point number equals HIP1012A pin number.

FIGURE 36. SCHEMATIC FOR +5V AND +12V OPERATION

HIP1012A (+5V and 12V) Figures (Continued)

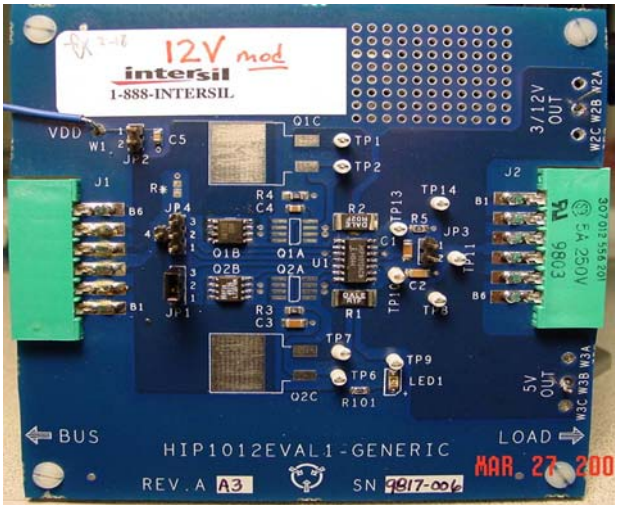


FIGURE 37. +5V AND +12V EVAL BOARD PICTURE

ISL6173 (+3.3V and +2.5V)

Figure 38 shows the ISL6173 dual low voltage Hot Swap controller. This IC targets applications between +2.1V and +3.6V for +Vin1, with a second channel controlling applications from +0.7V to +Vin1. The ISL6173 is biased via +Vin1. For the following measurements, channel 1 will control +3.3V, and channel 2 +2.5V.

Both Figures 41 and 42 show the device turning on due to the enable lines being asserted (forced low). Figure 41 shows each output in a soft-start ramp up after being enabled, while Figure 42 shows more detail regarding only channel 1 (+3.3V in this case) during soft-start.

Figures 43 and 44 show an OC condition occurring during operation on channel 1 (+3.3V). The device enters CR mode until CT1 times out, at which point the switch on channel 1 latches off. In Figure 44, note that (PG1)' is triggered upon VO1 dipping, while (FLT1)' stays high until CT1 times out. The nominal time-out for this device is (CTIM*1.178)/10µA.

Both Figures 45 and 46 show an OC condition occurring during operation on channel 1 (+3.3V). Figure 45 shows the gate signal and output voltage of channel 2 staying high while channel 1 shuts down. Figure 46 shows the Power Good and Fault signals for each channel, again note that (PG1)' and (FLT1)' are tripped, while (PG2)' and (FLT2)' remain unaffected.

Figures 47 and 48 show an OC condition occurring during operation on channel 1 (+3.3V). The device enters CR mode but the load recovers before CT1 has a chance to time out. Notice that (PG1)' is triggered with the dip in VO1, then recovers, while (FLT1)' stays high due to CT1 never timing out. The nominal time-out for this device is (CTIM*1.178)/10µA.

In Figure 49, the ISL6173 is in reset mode, which means the device will attempt to bring up channel 1 again after discharging CT1 64 times. This process will repeat infinitely.

In the case of high di/dt shorts, a WOC condition exists (see Figure 65). The controller will immediately pull GT to GND before attempting to enter CR mode. Note that the load is released before timeout occurs here.

Both channels are disabled by bringing their respective enable lines high (see Figure 66).

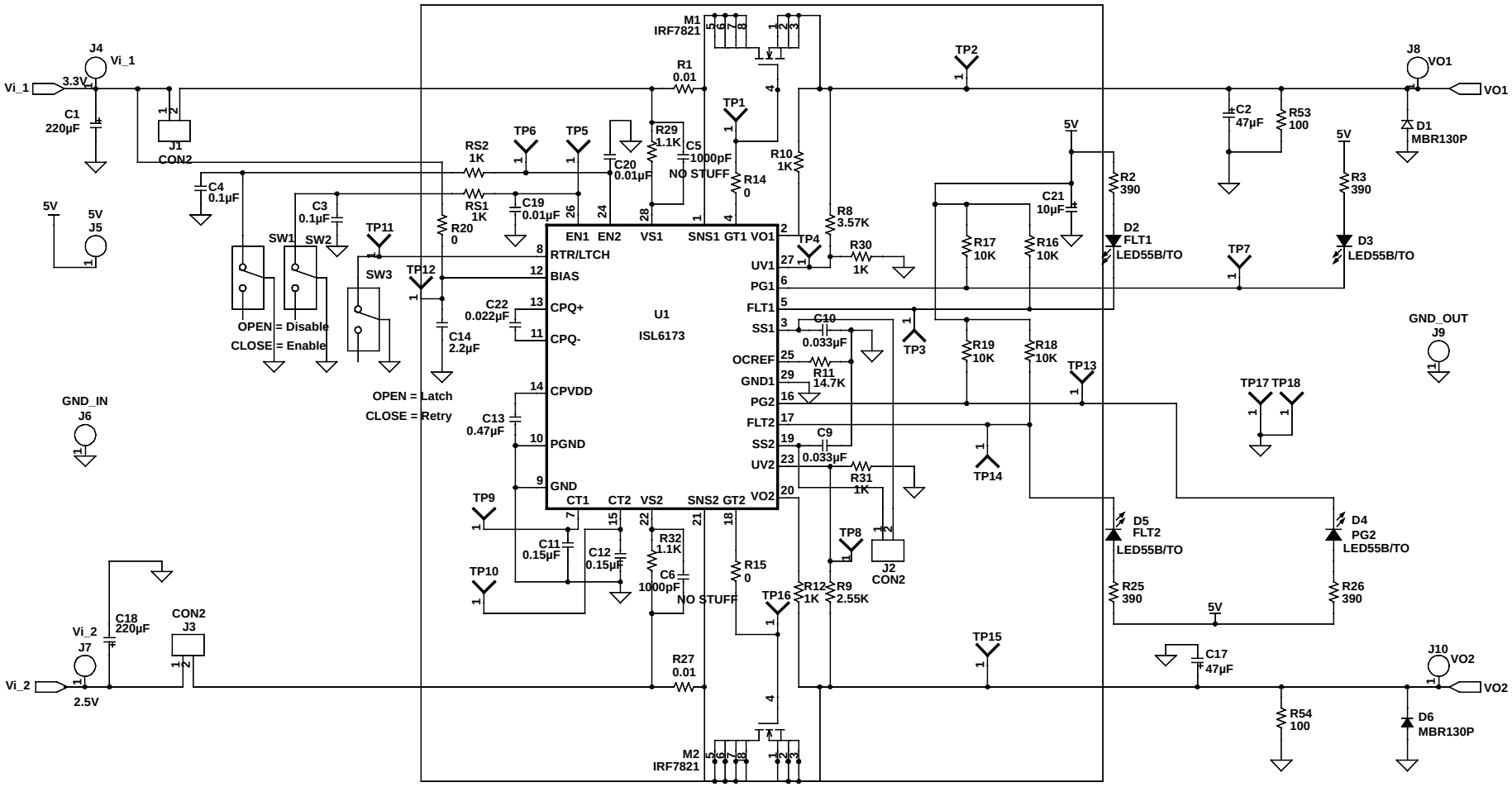


FIGURE 38. EVAL BOARD SCHEMATIC

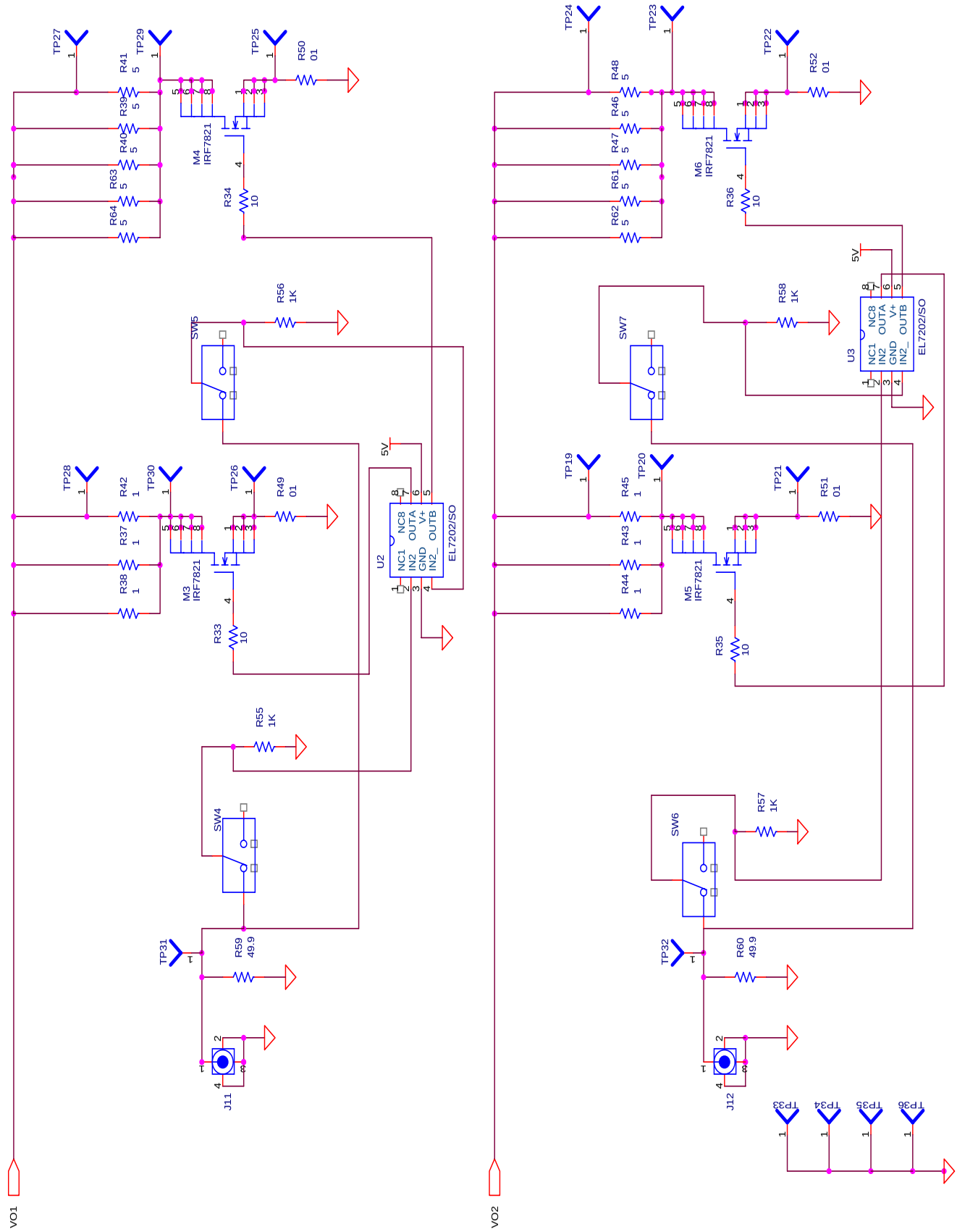


FIGURE 39. EVAL BOARD SCHEMATIC (CONTINUED)

ISL6173 (+3.3V & +2.5V) Figures

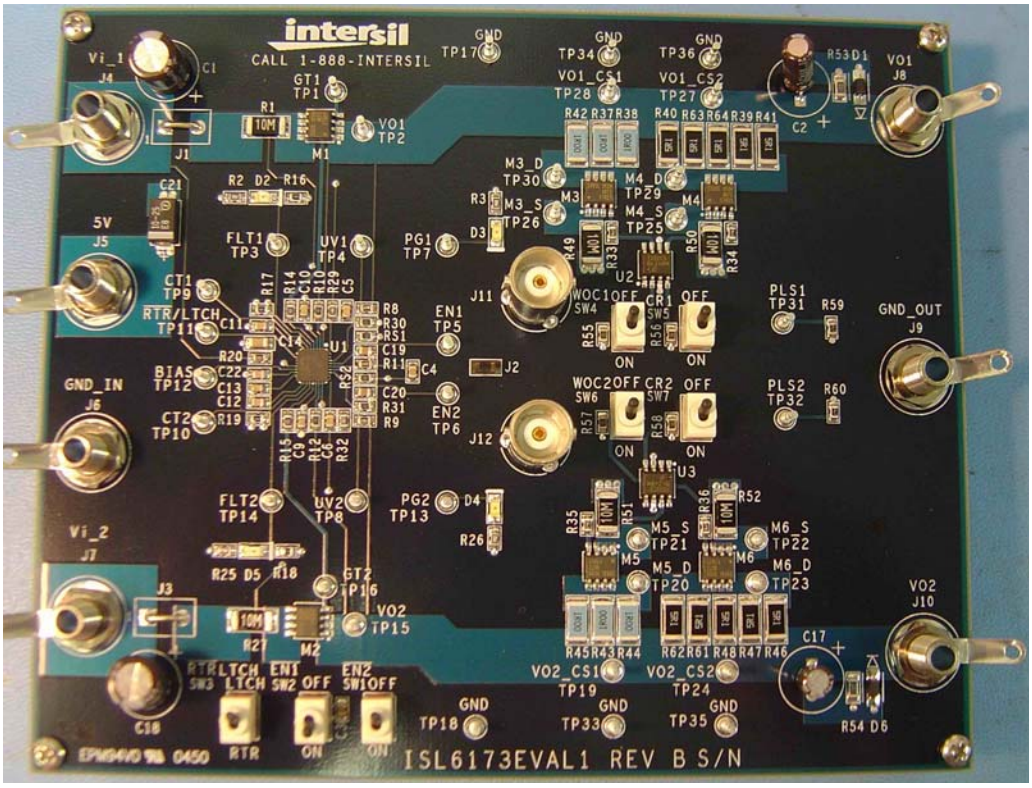


FIGURE 40. ISL6173 EVAL BOARD PICTURE

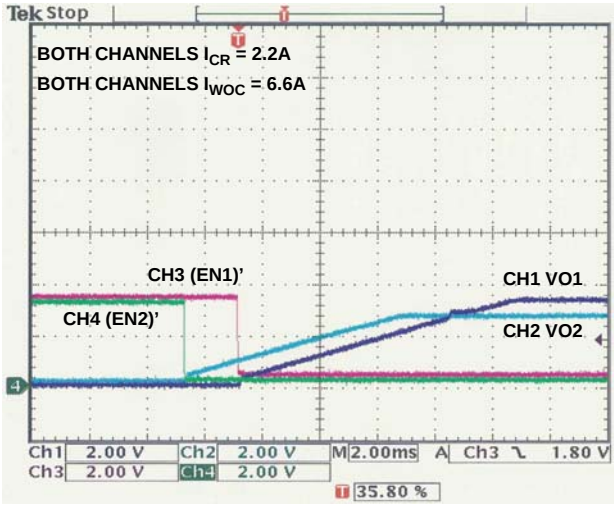


FIGURE 41. TURN ON VIA (EN)' SHOWING BOTH CHANNELS

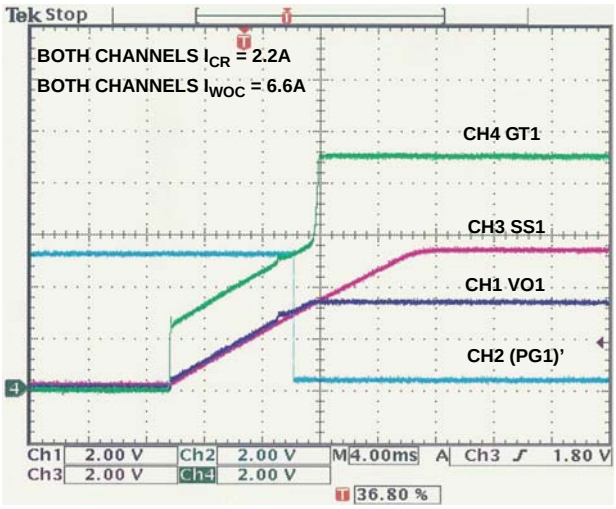


FIGURE 42. TURN ON SHOWING CHANNEL 1 DETAILS

ISL6173 (+3.3V & +2.5V) Figures (Continued)

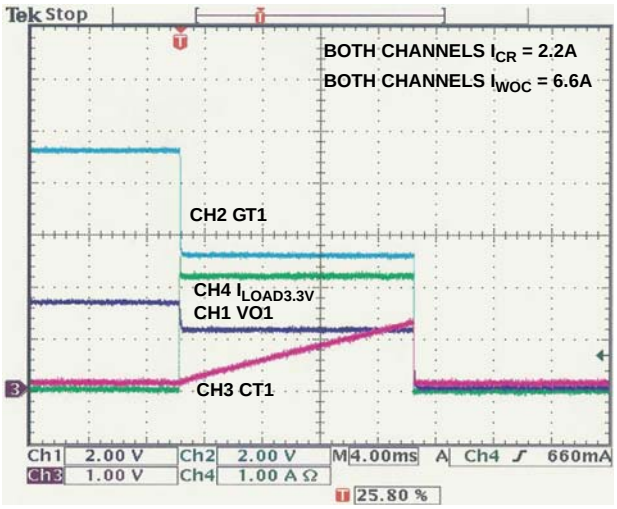


FIGURE 43. RESPONSE TO OC IN LATCH MODE (CT)

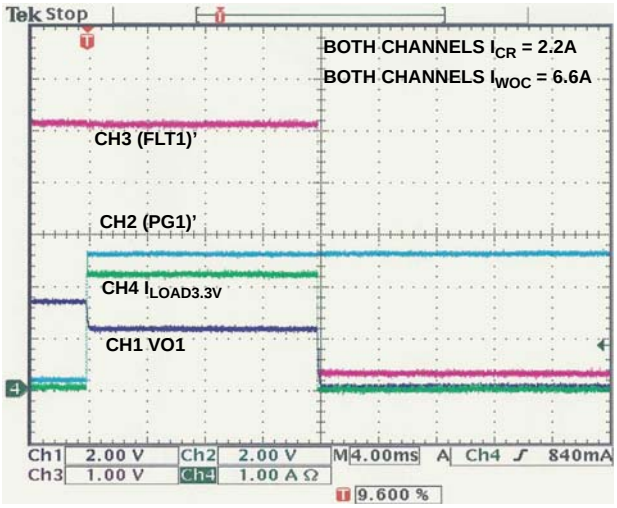


FIGURE 44. RESPONSE TO OC IN LATCH MODE ((PG)')

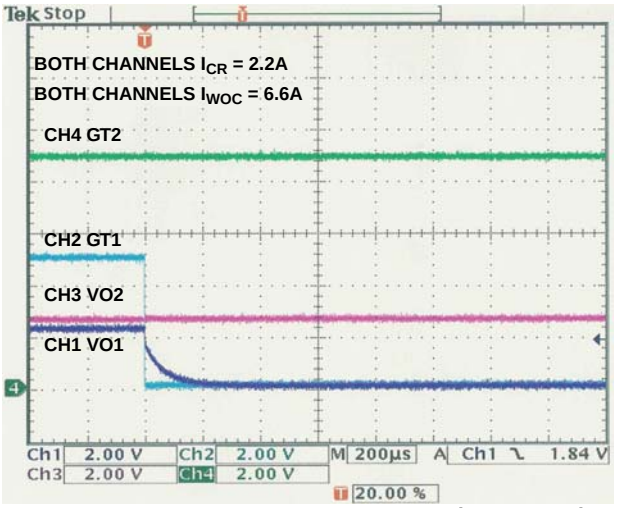


FIGURE 45. OC CHANNEL COMPARISON (VO AND GT)

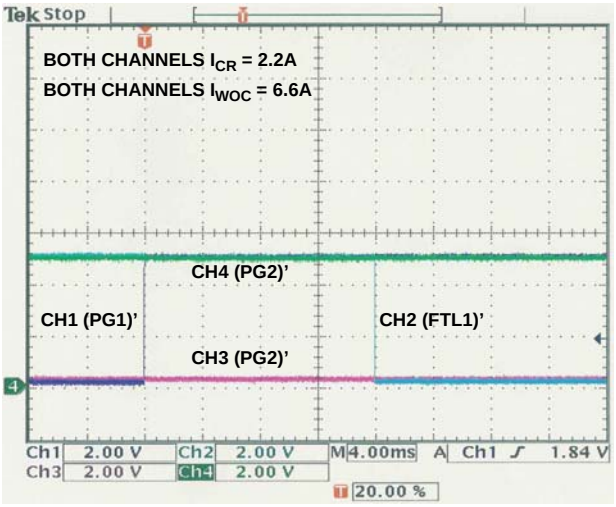


FIGURE 46. OC CHANNEL COMPARISON ((FLT)' AND (PG)')

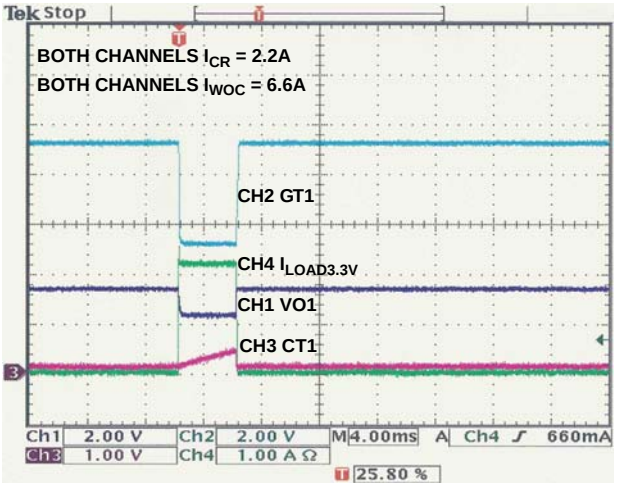


FIGURE 47. OC WITH RECOVERY BEFORE TIMEOUT (CT)

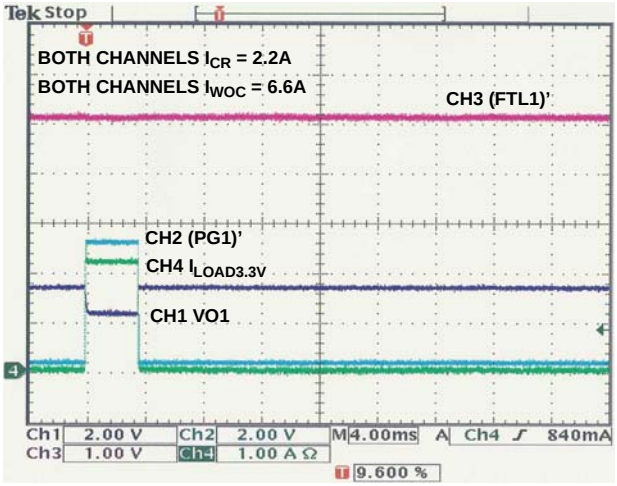


FIGURE 48. OC WITH RECOVERY BEFORE TIMEOUT ((PG)')

ISL6173 (+3.3V & +2.5V) Figures (Continued)

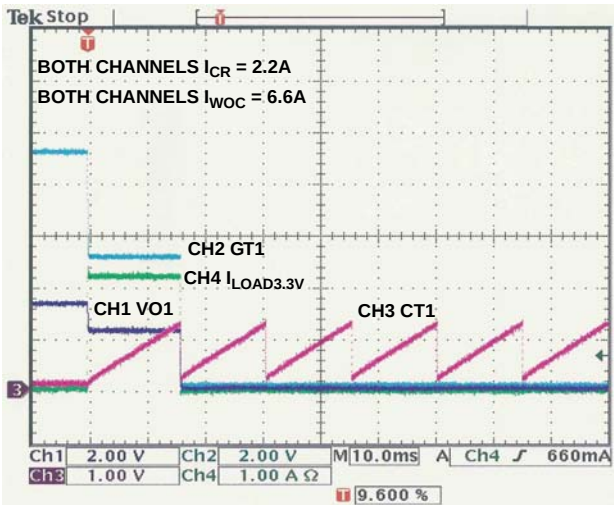


FIGURE 49. OC IN RESET MODE

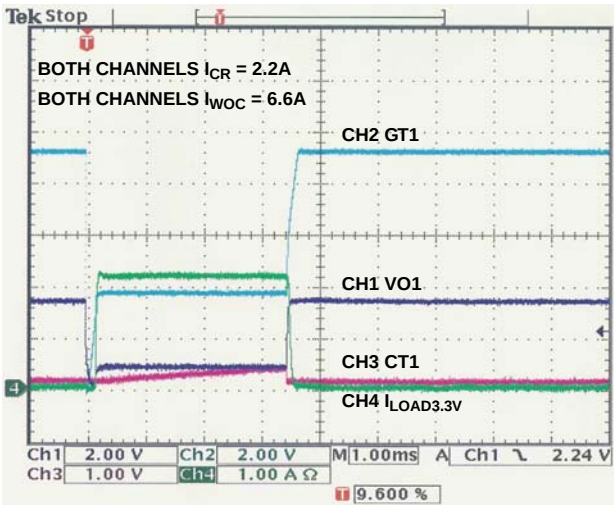


FIGURE 50. RESPONSE TO WOC

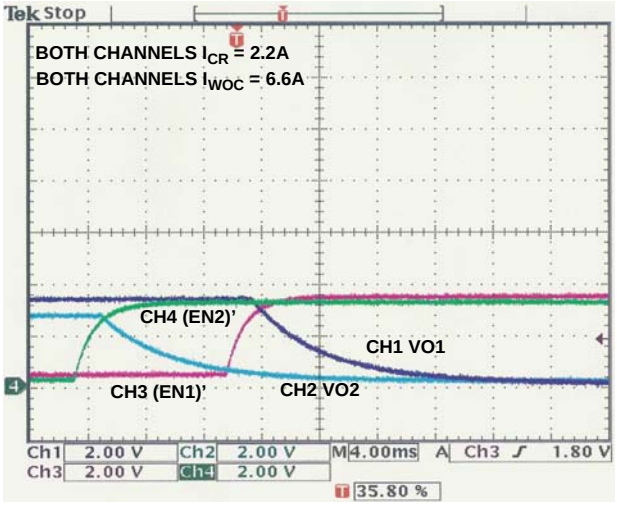


FIGURE 51. TURN OFF VIA (EN)'

ISL6111 (+12V, -12V, +3.3V, +5V)

Figures 52 and 53 show the ISL6111 PCI Hot Plug power switch controller. This IC provides power control for the four legacy supplies (+12V, -12V, 3.3V, 5V) to a PCI or PCI-X slot. The +12V and -12V switches are integrated, while the higher power 3.3V and 5V lines require external N-channel FETs.

Refer to Figures 54 and 55. Though on different time scales, both figures show the same event; Figure 54 shows all four output voltages ramping up, and Figure 55 gives detailed information pertaining to a single rail (+3.3V) at startup. There is a 1Ω resistive load on the +3.3V output.

Refer to Figures 56 and 57. Though on different time scales, both figures show the same event; Figure 56 shows all four output approaching GND, and Figure 57 gives detailed information pertaining to a single rail (+3.3V) at shutdown by EN. There is a 1Ω resistive load on the +3.3V output.

Both Figures 58 and 59 show the same event, each with a different set of details. Note that PGOOD goes low as soon as 3.3VS drops, but FLTLN waits until CR mode has expired. The nominal time-out period for this device is CTIM x 150kΩ.

Turning on into a direct short, the +3.3V section of the controller goes immediately into CR mode until CRTIM times out. The nominal time-out period for this device is CTIM x 150kΩ (see Figure 46).

ISL6111 (+12V, -12V, +3.3V, +5V) Figures

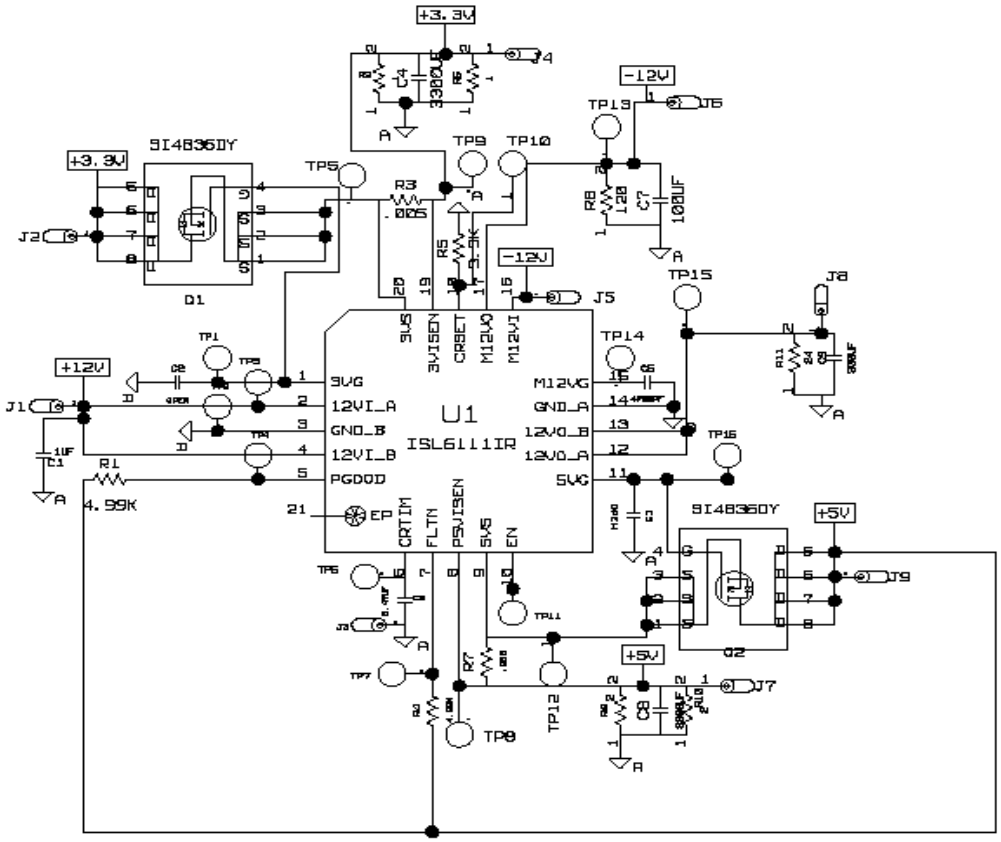


FIGURE 52. EVAL BOARD SCHEMATIC

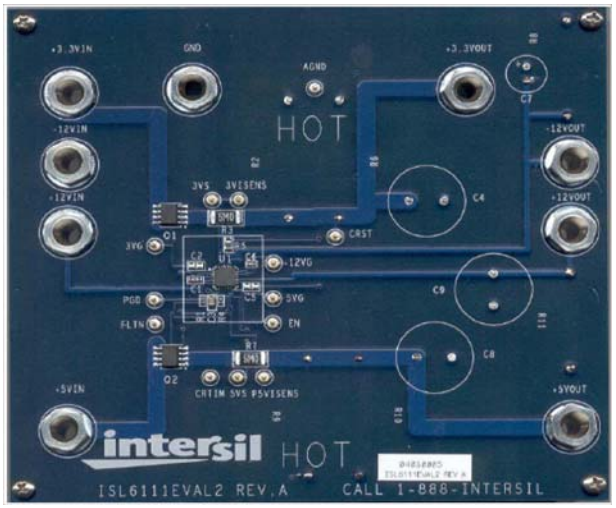


FIGURE 53. EVAL BOARD PICTURE

ISL6111 (+12V, -12V, +3.3V, +5V) Figures (Continued)

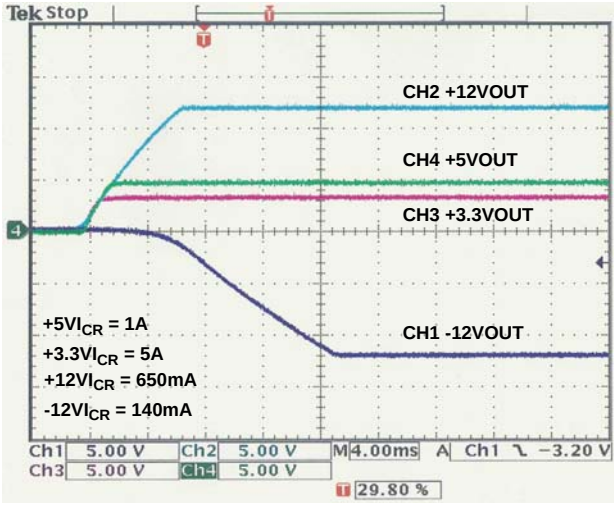


FIGURE 54. TURN ON SHOWING ALL OUTPUTS

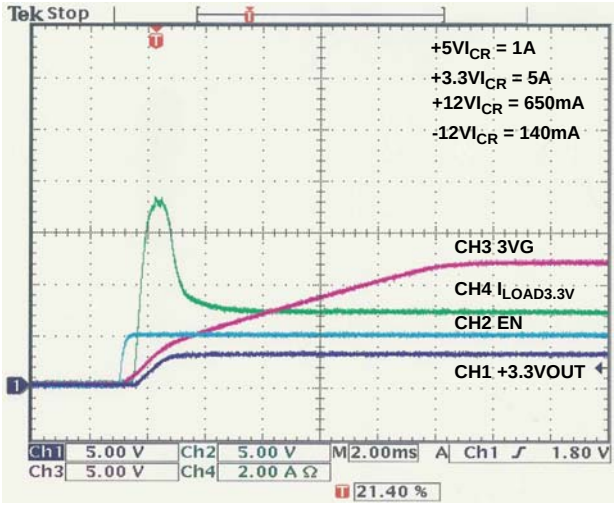


FIGURE 55. TURN ON SHOWING +3.3V DETAILS

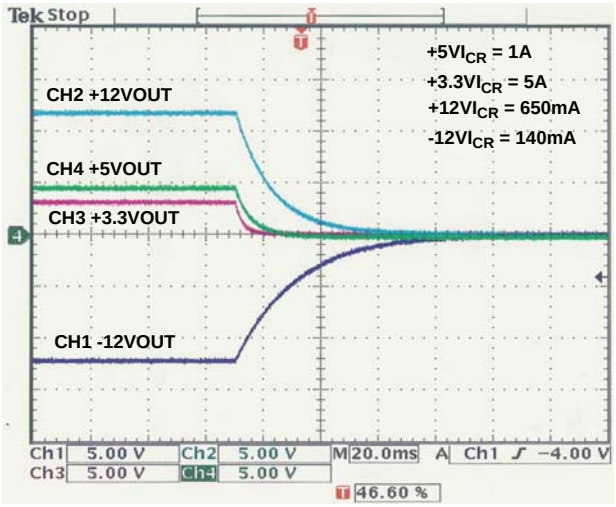


FIGURE 56. TURN OFF SHOWING ALL OUTPUTS

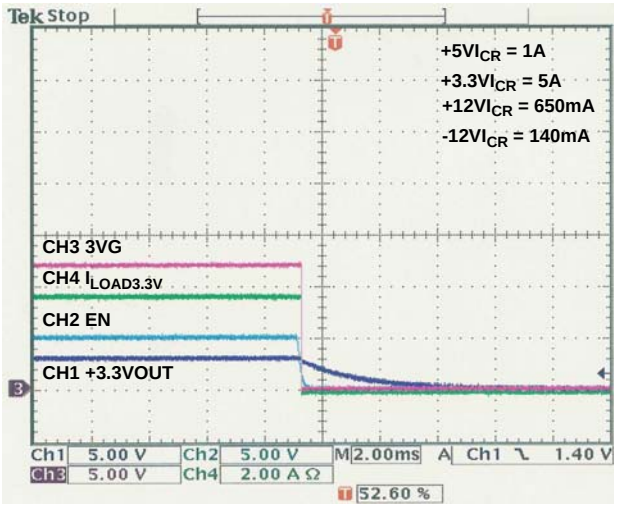


FIGURE 57. TURN OFF SHOWING +3.3V DETAILS

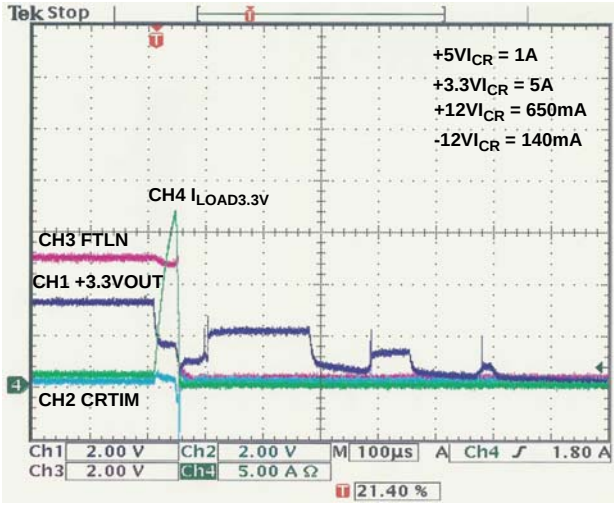


FIGURE 58. RESPONSE TO OC ON +3.3V CHANNEL

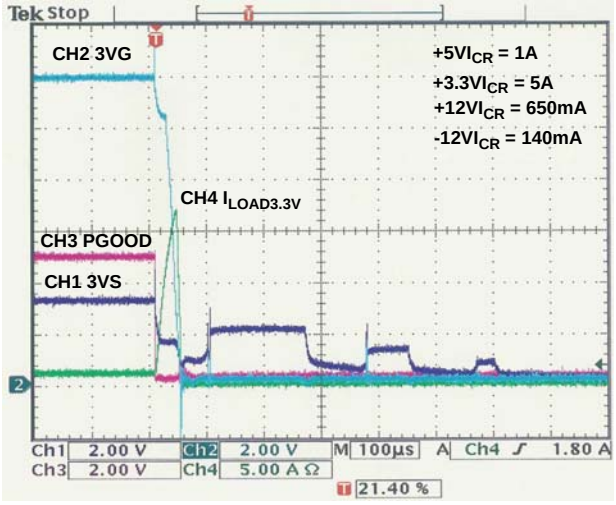


FIGURE 59. RESPONSE TO OC ON +3.3V CHANNEL

ISL6111 (+12V, -12V, +3.3V, +5V) Figures (Continued)

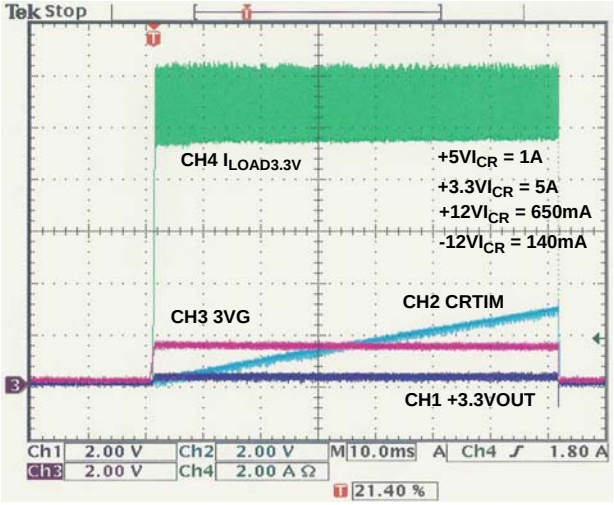


FIGURE 60. TURN ON INTO SHORT ON +3.3V

ISL6118 (+5V x2)

Figures 61 and 62 show the ISL6118 dual power supply controller. This IC provides fully independent OC fault protection for the +2.5V to +5.5V environment, with integrated MOSFETs. For ease of testing, EN1 and EN2 were tied together on this board.

Refer to Figures 63 and 64. After EN is asserted, notice the soft-start ramp of both outputs to VIN, in this case +5V. Also notice that $\overline{\text{FAULT2}}$ is only an indicator of an OC timeout, thus is not an indicator of under voltage conditions.

Figure 65 shows an OC condition occurring through channel 2 of the IC. Note that channel 1 stays up regardless of the condition of channel 2. Figure 66 shows turning on into an OC condition on channel 2. Again, channel 1 is unaffected.

ISL6118 (+5V x2) Figures

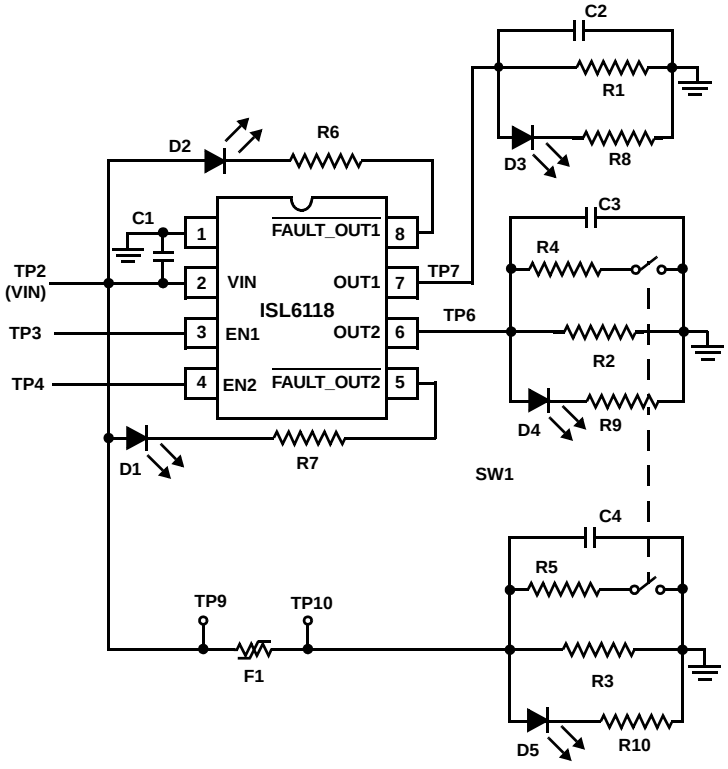


FIGURE 61. EVAL BOARD SCHEMATIC

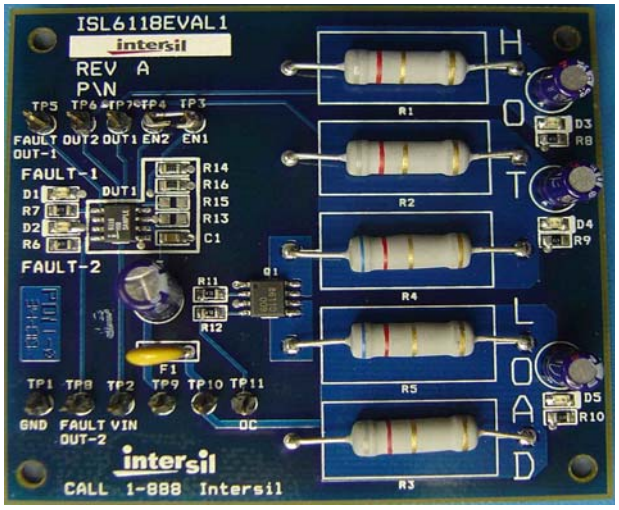


FIGURE 62. EVAL BOARD PICTURE

ISL6118 (+5V x2) Figures (Continued)

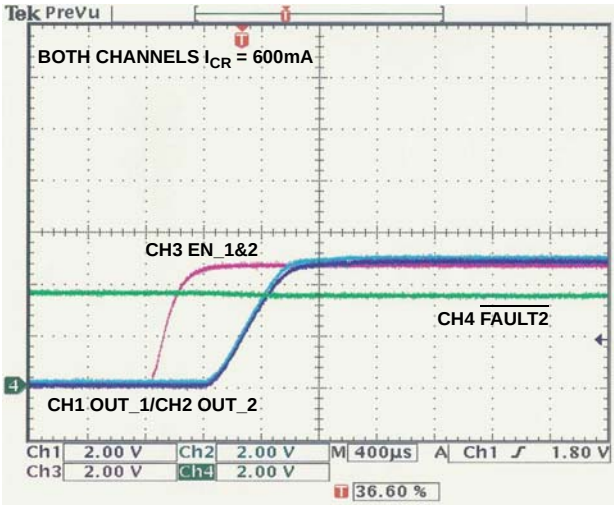


FIGURE 63. TURN ON VIA EN

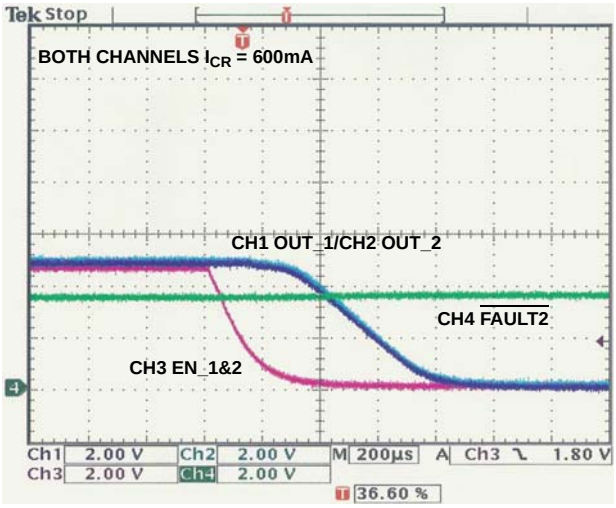


FIGURE 64. TURN OFF VIA EN

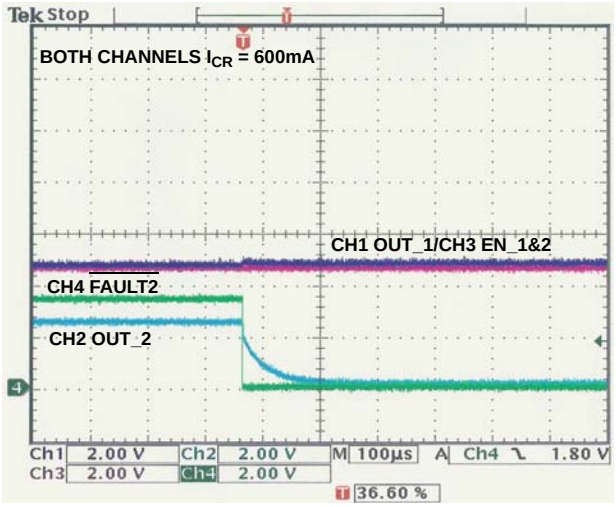


FIGURE 65. RESPONSE TO OC CONDITION

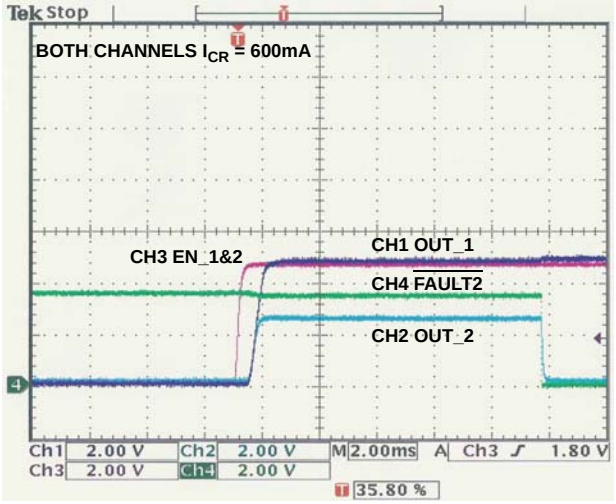


FIGURE 66. TURN ON INTO SHORT

Setting the Overcurrent Trip Point

Setting Hot Plug Over Current Trip Points

In general, Intersil hot plug devices sense load current through a sense resistor, then compare the voltage generated across this sense resistor to a voltage programmed via a “set” resistor

Steps to Set OC Trip Point: (Steps may vary slightly by part)

1. Select desired OC trip point level
2. Determine R_{ISET} by selecting sense threshold voltage to design to
3. Calculate R_{ISENSE} based on OC level selected in step 1

HIP1012A, ISL6115, ISL6116 Devices

To set HIP1012A, ISL6115, and ISL6116 CR levels, use the equation:

$$R_{ISENSE} = \frac{V_{th}}{I_{OC}}$$

With:

HIP1012A

$$V_{th} = R_{ISET} \bullet 10\mu A$$

R_{ISET} RESISTOR (Ω)	NOMINAL OC VTH (mV)
10k	200
4.99k	100
2.5k	50
750	15

Or

ISL6115, ISL6116

$$V_{th} = R_{ISET} \bullet 20\mu A$$

R_{ILIM} RESISTOR (kΩ)	NOMINAL OC VTH (mV)
15	150
10	100
7.5	75
4.99	50

For PCI Applications:

Set R_{CRSET} to 4.22kΩ, which provides a nominal current trip level 110%-130% higher than maximum specified PCI range

For Non-PCI Applications:

Do NOT use R_{CRSET} > 15kΩ (thermal considerations)

Do select R_{CRSET} > 3.0kΩ to avoid noise faults

SUPPLY (V I_{CR})	NOMINAL CURRENT REGULATION LEVEL (10%) FOR EACH SUPPLY
+3.3	((100µA x R_{CRSET})/8.54)/R_{RSENSE}
+5.0	((100µA x R_{CRSET})/12)/R_{RSENSE}
+12	(100µA x R_{CRSET})/0.7
-12	(100µA x R_{CRSET})/3.3

ISL6173 (+3.3V and +2.5V)

To set ISL6173 CR level, use the equation:

$$I_{CR} = \frac{(I_{SET} \bullet R_{SET})}{I_{SNS}}$$

Where:

$$I_{SET} = \frac{I_{REF}}{4} \text{ and } I_{REF} = \frac{V_{OCREF}}{R_{OCREF}}$$

$$I_{REF} = (\text{typically } 80\mu A)$$

ISL6118

The ISL6118 current sense and limiting circuitry sets the current limit to a nominal 600mA.

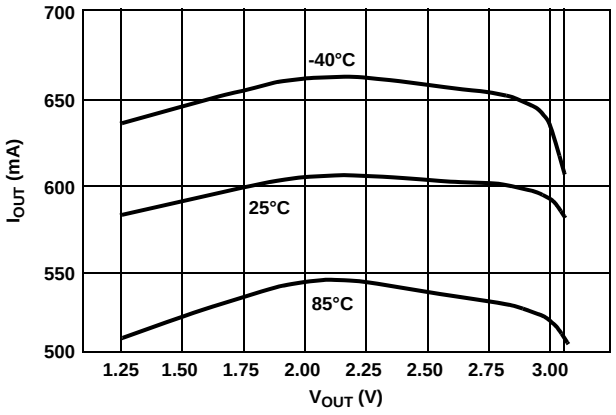


FIGURE 67. CURRENT REGULATION vs V_{OUT} (V_{IN} = 3.3V)

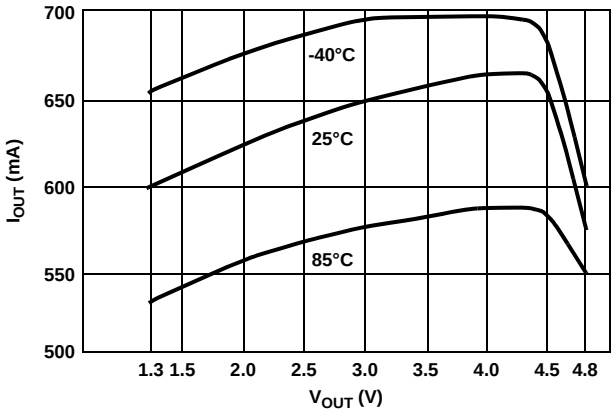


FIGURE 68. CURRENT REGULATION vs V_{OUT} (V_{IN} = 5V)

Summary of Overcurrent Response

HIP1012A - If programmed OC setpoint is exceeded, gate is modulated to regulate current to current regulation level until programmed timeout occurs. If timeout occurs, both gates latch off. If the load current exceeds 300% of the programmed OC setpoint, affected gate is immediately pulled to ground, then modulated to regulate current to current regulation level until timeout occurs.

HIP1013 - If OC setpoint is exceeded, both gates will latch off ~2µs after OC event

HIP1011, A, B, D, E - If programmed OC setpoint is exceeded, all outputs latch off.

ISL6115, ISL6116, ISL6117, ISL6120 - If programmed OC setpoint is exceeded, gate is modulated to regulate current to current regulation level until programmed timeout occurs. If timeout occurs, the gate latches off. If the overcurrent voltage threshold is exceeded by more than 150mV, the affected gate is immediately pulled to ground, then modulated to regulate current to current regulation level until timeout occurs.

ISL6118, ISL619, ISL6121 - If OC setpoint is exceeded, current is regulated then the gate latches off ~12ms after OC event.

ISL6111 - If programmed OC setpoint is exceeded, gate is modulated to regulate current to current regulation level until programmed timeout occurs. If timeout occurs, all four gates latch off.

HIP1020 - This device does not provide current monitoring.

ISL6140, ISL6150 - If programmed OC setpoint is exceeded for more than 2µs, gate will latch off.

ISL6173 - Two levels of overcurrent detection are present, CR mode and WOC (Way Overcurrent) mode. If load current reaches OC setpoint, the gate is modulated to regulate current to current regulation level until current drops below CR or programmed timeout occurs. If timeout occurs, output will either latch off or indefinitely retry depending on condition of $\overline{\text{RTR}}$/LTCH pin. WOC mode is reached upon a very high di/dt spike of >300% CR. Gate is pulled to GND immediately, then the device enters CR mode.

ISL6141/51 - If programmed OC setpoint is exceeded, gate is modulated to regulate current to current regulation level until 500µs timeout occurs. If the overcurrent voltage threshold is exceeded by more than 150mV, the affected gate is immediately pulled to ground, then modulated to regulate current to current regulation level until 500µs timeout occurs. If timeout occurs, the gate latches off.

ISL6142/52 - If programmed OC setpoint is exceeded, gate is modulated to regulate current to current regulation level until programmed timeout occurs. If the overcurrent voltage threshold is exceeded by more than 150mV, the affected gate is immediately pulled to ground, then modulated to regulate current to current regulation level until programmed timeout occurs. If timeout occurs, the gate latches off.

ISL6161 - If programmed OC setpoint is exceeded, gate is modulated to regulate current to current regulation level until programmed timeout occurs. If timeout occurs, both gates latch off. If the load current exceeds 300% of the programmed OC setpoint, affected gate is immediately pulled to ground, then modulated to regulate current to current regulation level until timeout occurs.

Hot Plug/Hot Swap Target Applications

HOT SWAP/HOT PLUG			TARGET APPLICATIONS						
INTERSIL PART NUMBER	BIAS VOLTAGE (V)	CONTROLLED VOLTAGE(S) (V)	PCI	COMPACT PCI	STORAGE SYSTEMS	-48V TELECOM	USB	INFINIBAND	GENERAL PURPOSE
HIP1011	+12	+12, -12, +5, +3.3	Y	Y					
HIP1011A	+12	+12, -12, +5, +3.3	Y	Y					
HIP1011B	+12	+12, -12, +5, +3.3	Y	Y					
HIP1011D	+12	+12, -12, +3.3, +5 x2	Y						
HIP1011E	+12	+12, -12, +3.3, +5 x2	Y						
HIP1012A	+12	+12/+5 or +5/+3.3			Y				
HIP1013	+12	+12/+5 or +5/+3.3			Y				
HIP1020	+12 to +5	+12/+5/+3.3 or +5/+3.3			Y				Y
ISL6111	+12	+12, -12, +5, +3.3	Y	Y	Y				
ISL6115	+12	+12			Y				Y
ISL6116	+12 or -V	+5 or -V			Y	Y			Y
ISL6117	+12	+3.3			Y	Y			Y
ISL6118	+2.5 to +5.5	2.5 to 5.5	Y				Y		Y
ISL6119	+2.5 to +5.5	2.5 to 5.5					Y		Y
ISL6120	+12	+2.5				Y			Y
ISL6121	+2.5 to +5.5	2.5 to 5.5			Y		Y		Y
ISL6140/50	-10 to -80	-10 to -80				Y			Y
ISL6141/51	-20 to -80	-20 to -80				Y			Y
ISL6142/52	-20 to -80	-20 to -80				Y			Y
ISL6160	+12 and +5	+12/+5						Y	Y
ISL6161	+12	+12/+3.3	Y						Y
ISL6173	+2.1 to +3.6	+2.17 to +3.6, +0.7 to VBIAS							

List of Figures